[0021] The doping of the fullerenes constituting the doped fullerene layer **3** is in the concentration of 10^{21} per cm^3 or one Li atom per C60. Li@C60 is an n-type material. However, experimental results to be described shortly demonstrate that Li@C60 in the aforementioned concentration is surprisingly metallic in behavior. More surprisingly, experimental results to be described shortly demonstrate that the doped/undoped fullerene junction of the diode hereinbefore described exhibits an I/V curve which is characteristic of a diode. In operation, the undoped fullerene layer **2** is connected to the anode of the diode and the doped fullerene layer **3** is connected to the cathode of the diode. This demonstrates that electronic devices can be fabricated based on junctions between metal doped fullerenes and undoped fullerenes. The metal doped fullerenes alone exhibit metallic properties and the undoped fullerenes alone exhibit semiconductor properties.

[0022] In other embodiments of the present invention, the undoped fullerene layer **2** may also be a monolayer. Similarly, in other embodiments of the present invention, the undoped fullerene layer **2** may be more than two molecules thick. Likewise, in other embodiments of the present invention, the doped fullerene layer **3** may be more than one molecule thick. In alternative embodiments of the present invention, different fullerenes may be employed, such as C82, for example. As indicated earlier, the doping of the fullerenes constituting the doped fullerene layer **3** is in the concentration of 1 Li atom per C60. However, different concentrations of electron donors may be employed in other embodiments of the present invention. Doping with more than one atom per C60 is equally possible. Other metals may be employed together with or in place of Li. Group 1 elements such as sodium (Na), potassium (K), otherwise known as the alkali metals, and elements such as lanthanum (La) are examples of possible alternatives. It will be appreciated then that Fermi levels and other relevant energy levels can be tuned by choice of dopant. Different combinations of endohedral and exohedral fullerenes are also possible in the interests of tuning barrier heights, carrier concentrations and transport properties.

[0023] The metal substrate **1** may be replaced by a semiconducting substrate such as a silicon substrate or an insulating substrate such as silicon dioxide substrate, with appropriate conductive contacts made to the undoped fullerene layer **2**. Examples of such contacts may be provided by intervening metal depositions, vias, or regions of degenerate semiconductor. The fullerenes can be located in step sites on such substrates. This advantageously permits self-assembly of devices. By surface relief patterning of the substrate, such devices can then be attached and interconnected at kinks, corners and steps in the pattern. As indicated earlier, Li@C60 is an n-type material. However, the present invention equally contemplates doping fullerenes with electron acceptors to produce p-type materials.

[0024] Such junctions as those described herein are important elements of nanoscale semiconductor technology. Possible applications of junctions such as those hereinbefore described include but are not limited to electronic and optoelectronic components such as diodes, photodiodes and the like on a nanometer scale. Such elements permit fabrication of many different well-known electronic devices, such as charge-coupled devices for example, at a much higher integration density than hitherto possible.

[0025] Referring now to **FIG. 2, a** junction field effect transistor (JFET) embodying the present invention comprises a silicon substrate **10**. An undoped fullerene layer **11** is deposited on the substrate **10**. A doped n-type fullerene layer **13** is deposited on the undoped fullerene layer **11**. A metal layer **12** is also deposited on the undoped fullerene layer **11**. The doped fullerene layer **13** is patterned to form a gate region G isolated from the metal layer **12** but in contact with the underlying undoped fullerene layer **11**. Similarly, the metal layer **12** is patterned to form a source region S and drain region D disposed on opposite sides of the gate region **13**. Both the source region S and the drain region D are in contact with the underlying undoped fullerene layer **11**. In operation, a charge conduction channel between the source S and the drain D is provided by the undoped fullerene layer **11**. Passage of charge between the source S and the drain D is controlled by application of control voltage to the gate region G. The voltage applied to the gate region G controls the extent to which a current limiting "pinch off" field extends into the undoped fullerene layer **11** beneath the gate region G.

[0026] Referring now to **FIG. 3**, another JFET embodying the present invention also comprises a silicon substrate **20**. A metal layer **21** is deposited on the silicon substrate **20** and patterned to provide a source region S and a drain region D disposed on opposite sides of an intervening aperture **22**. An undoped fullerene layer **23** is deposited on the substrate **20** in the aperture **22**. A doped n-type fullerene layer **24** is deposited on the undoped fullerene layer **23**. The doped fullerene layer **24** is patterned to form a gate region G isolated from the source S and the drain D. In operation, a charge conduction channel between the source S and the drain D is again provided by the undoped fullerene layer **23**, and passage of charge between the source S and the drain D is again controlled by application of control voltage to the gate region G, as hereinbefore described with reference to **FIG. 2**.

[0027] In the JFETs hereinbefore described with reference to **FIGS. 2 and 3**, the undoped fullerene layer is formed from C60. The doped fullerene layer is a monolayer formed from Li@C60. The doping of the fullerenes constituting the doped fullerene layer **3** is in the concentration of 1 Li atom per C60. The thickness x of the gate region G is one monolayer. The gate region in plan view is a square of side in the region of 10 nm (10 molecules).

[0028] In other JFETs embodying the present invention, a different fullerene may be employed, such as C82, for example. Similarly, in other JFETs embodying the present invention, other dopant metals may be employed together with or place of Li. Group 1 elements such as Na, K, otherwise known as the alkali metals, and elements such as La, are examples of possible alternatives. Likewise, different concentrations of electron donors may be employed in other embodiments of the present invention. It should also be realized that, in other JFETs embodying the present invention, the gate region may be greater than one monolayer thick. Similarly, in other JFETs embodying the present invention, the gate region may have a different shape and dimensions to those hereinbefore described with reference **FIGS. 2 and 3**. Also, in other JFETs embodying the present invention, the undoped fullerene layer may be greater than one molecule thick.